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Selective Harmonic Elimination in Cascaded Multilevel Inverters using Imperialist Competitive Algorithm

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Abstract

In this paper, for Selective Harmonic Elimination (SHE) in cascaded multi-level inverters and reaching optimal switching angles to eliminate low-level harmonics in output waveform, Imperialist Competition Algorithm (ICA) is used. ICA is implemented on 7-level and 11-level inverters so that optimal switching angles are achieved by solving formed non-linear equations. ICA is a general searching strategy with socio-political stimulus which was introduced to solve different optimization problems and has more accuracy and faster convergence compared to similar algorithms. Results obtained from ICA will be compared with GA and this method is superior in achieving general minimum amount and having more convergence rate. To investigate analyses and simulation results, an experimental sample of inverter in an empirical study will be presented, as well.

Keywords: SHE, Cascaded Multi-Level Inverters, Optimal Switching Angles, ICA.

1. Introduction

Using power electronic converters has expanded along with increasing development of renewed energies. Using multi-level inverters as a connector in these systems is growing. In high power and middle voltage applications, multi-level inverters have been paid more attention than contradiction two-level inverters due to their low switching losses, high efficiency and high electromagnetic adaptability. In recent years, works related to this subject are as following:

A new method is presented based on Firefly Algorithm to select optimal switching angles [1]. Equations obtained from general harmonic distortions in output voltage of cascaded multi-level inverters are considered as Objective Function. This objective function was used to minimize Total Harmonic Distortion (THD) in output voltage of a multi-level inverter.

To eliminate selective harmonics in cascaded multi-level inverters, using Particle Swarm Optimization (PSO) Algorithm is proposed [2]. The proposed method in this article was used to solve problems with a new simpler way even if switching angles increases. Investigation of topologies, control methods and application of multi-level inverters including multi-level inverters of diode clip, multi-level inverters of flying capacitor and cascaded multi-level

inverters with independent dc resources and also introduction of new topologies such as multi-level inverters with asymmetric hybrid cells and multi-level inverters with switching approaches were presented [3].

Titled "Investigation of Multi-level Inverters" [4], it is proceeded to consider such inverters and in [5] titled "Elimination of Harmonics in Multi-level Converters with Uneven dc Resources", authors have investigated eliminating harmonics in such converters. In refer [6]; minimization of adaptive selective harmonics in cascaded multi-level inverters with variable dc resources is investigated using Artificial Neural Networks. Eliminate selective harmonics in seven-level inverters, SHEPWM technique is used to control modulation [7]. And [8] to eliminate selective harmonics based on Genetic Algorithm to solve non-algebraic and non-linear equations, minimization of harmonics in multi-level inverters is utilized using pulse width modulation technique. These equations determine switching angles which are used to minimize THD. In this paper, we will proceed to investigate structure and techniques of inverters, then formulation of problem and proposed algorithm and finally the studied system and its results.

2. Structure of multi-level inverters

In two recent decades, different topologies have been introduced for multi-level inverters and also in researches it has been dealt with new modulation methods and controlling strategies however three main structures can be introduced for multi-level inverters which in most articles they have been referred to:

1) Cascaded multi-level inverters with independent dc resources.
2) Multi-level inverters with diode clip.
3) Multi-level inverters with capacitor clip or flying capacitor

2.1. Cascaded multi-level inverters with independent dc resources

A cascaded multi-level H-bridge inverter includes a number of single-phase H-bridge inverters which are connected to each other in a cascaded manner and each is connected to an independent DC resource [9]. A schematic image of a cascaded H-bridge inverter is presented in Figure (1) which includes single-phase s inverter and number of its level comes from (2s + 1). Depending on state of keys, three levels of voltage can be attained in output of each inverter. With voltage $+V_{DC}$ (when S_1 and S_4 are on), voltage $-V_{DC}$(when S_2 and S_3 are on) and voltage 0 (when S_1 and S_3 or S_2 and S_4 are on), k = 1, 2… s, output voltage according to Equation (1) equals total of output voltage of each single-phase inverter:

$$v_o = v_1 + v_2 + \cdots + v_s \quad (1)$$

Output voltage waveform of an eleven-level inverter and output inverter of each single-phase inverter connected in a cascaded manner is presented in Figure (2).

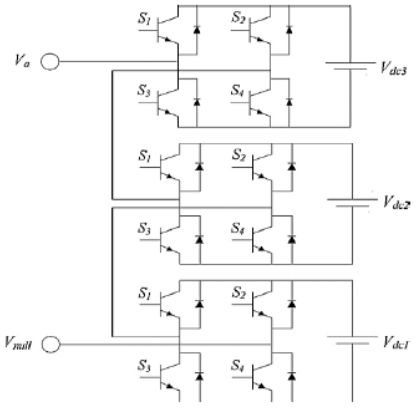

Figure 1. Cascaded multi-level inverter [9]

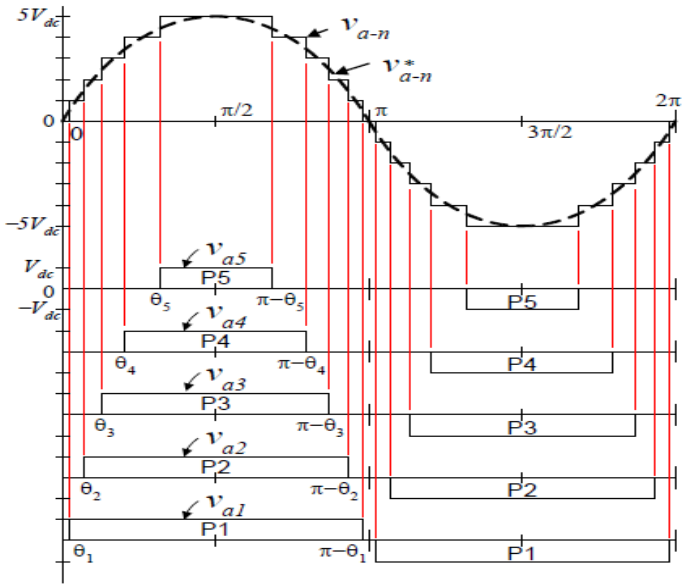

Figure 2. Output voltage waveform of a cascaded 11-level inverter and output voltages of inverters connected in a cascaded manner

2.2. Multi-level inverters with a diode clip

An m-level converter of diode clip includes (m – 1) capacitor over dc bus and produces m-level of phase voltage [10]. Figure (3) indicates a five-level inverter of single-phase complete bridge diode clip which dc bus includes four capacitors C_1, C_2, C_3 and C_4.The voltage passing each capacitor equals $V_{dc}/4$ and voltage stress on each key through diode clips will be limited to this voltage.

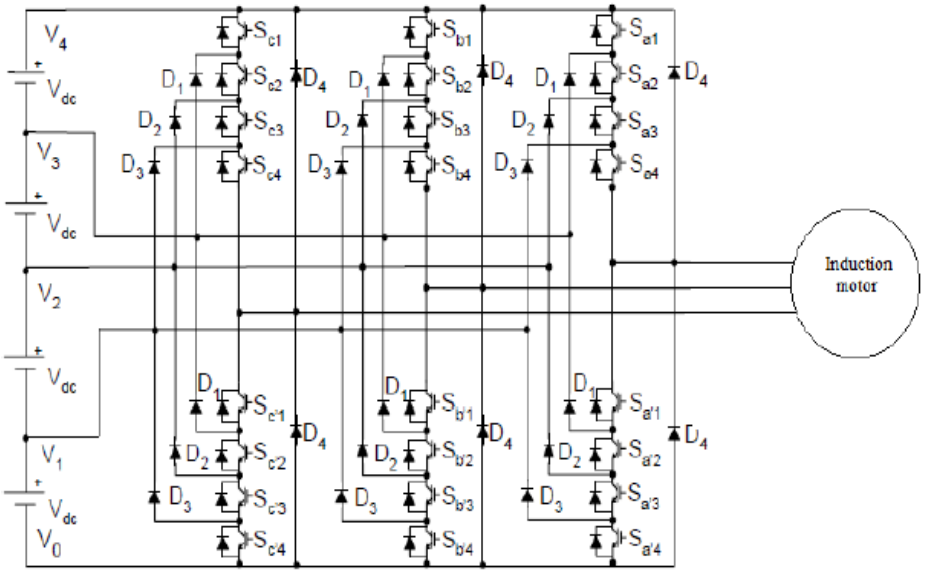

Figure 3. Structure of a five-level three-phase inverter based on diode clip [10]

Figure (4) indicates a phase and linear voltage waveform of a five-level inverter. Linear voltage includes a positive base of a phase and a negative base of b phase. Each phase voltage follows a half of Sinus Wave and finally linear voltage is a nine-level square waveform and this shows that a m-level inverter in output, makes a m-level phase voltage and a linear voltage with (2m – 1) level [10].

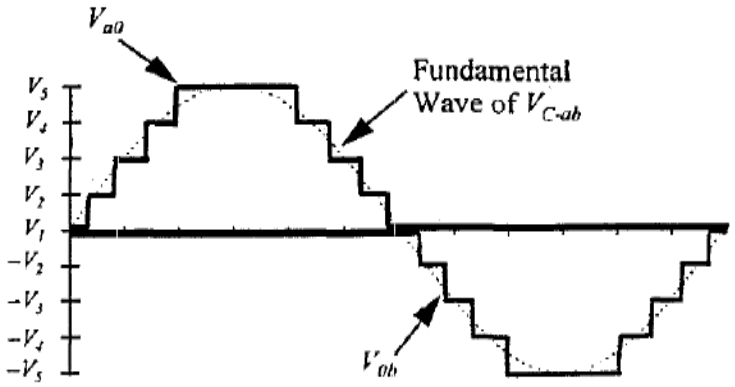

Figure 4. Waveform of linear voltage and phase voltage of a five-level diode-clip inverter [10]

2.3. Multi-level inverters with a capacitor clip or flying capacitor

Figure (5) shows a typical arrangement for a 5-level inverter with a flying capacitor [11]. This arrangement is obtained from arrangement of a two-level inverter adding permanent capacitors to cascaded keys. In each branch of inverter, four pairs of keys are placed with supplementary performance. For example, Branch A includes (S'_1, S_1) ، (S'_2, S_2) ، (S'_3, S_3) and (S'_4, S_4). Therefore, only four independent gate signals are required for each phase of inverter.

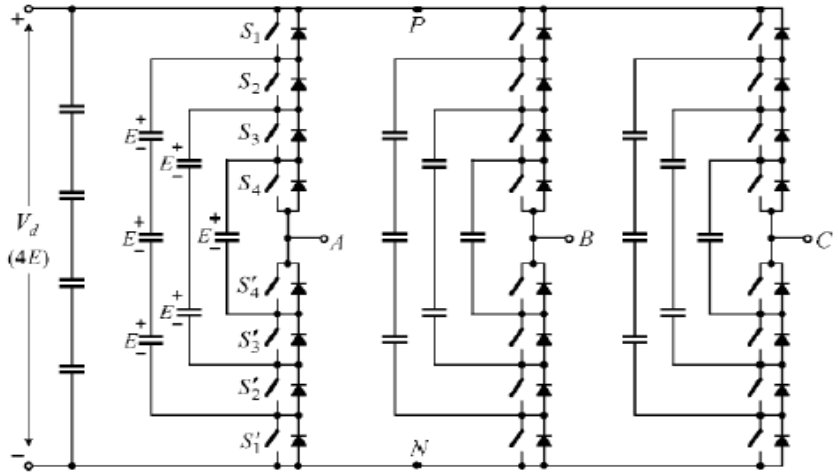

Figure 5. A five-level flying capacitor inverter [11]

3. Modulation techniques of multi-level inverters

The modulation methods used in multi-level inverters can be categorized in terms of switching frequency according to Figure (6) [3]:

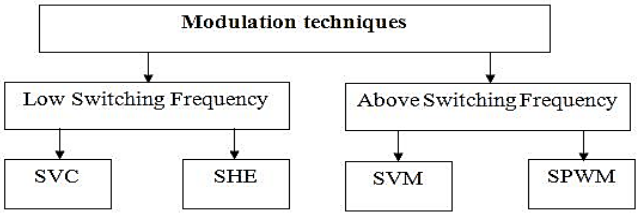

Figure 6. Modulation techniques classification of multi-level inverters

The methods working the above switching frequency, for power semiconductors in a cycle

of output voltage have high commutation. The methods working with low switching frequency generally in each cycle of output voltage for power semiconductors have one or two commutations and make a square waveform. At the rest, we consider SHE.

3.1. SHE

One of low-frequency harmonics elimination methods in output voltage range of an inverter is SHE technique [12]. This technique can be implemented on cascaded multi-level inverters. Output voltage has a stepped waveform and when keys are on one can eliminate dominant harmonics by selecting appropriate switching angles. For an m-level inverter with switching angles θ_k which $k = 1,2,3, \dots, s$ and $\theta_1 < \theta_2 < \theta_3 < \cdots < \theta_s$, in which S is number if input independent dc resources, one can eliminate s – 1 low-level harmonics by appropriately selecting. θ_k , For an eleven-level inverter by appropriately selecting switching angles, the dominant harmonics which one can eliminate include 5th, 7th, 11th and 13th harmonics. To achieve these switching angles, it is required that we form five 5-unknown equations which four of them are selected according to the selective harmonics which should be eliminated and the fifth equation is obtained according to the amount which the 1st harmonic should have compared to the reference amount, which amount of index of M modulation is gained from Relation (2):

$$\mathrm{M} = \frac{\pi V_1}{4sV_{dc}} \tag{2}$$

This amount is $0 \leq \mathrm{M} \leq 1$. In this equation, V_1 is the main component of output voltage of the inverter which is described according to Equation (3):

$$\begin{cases} \frac{1}{5}[\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4) + \cos(\theta_5)] = \mathrm{M} \\ \cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) + \cos(5\theta_4) + \cos(5\theta_5) = 0 \\ \cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) + \cos(7\theta_4) + \cos(7\theta_5) = 0 \\ \cos(11\theta_1) + \cos(11\theta_2) + \cos(11\theta_3) + \cos(11\theta_4) + \cos(11\theta_5) = 0 \\ \cos(13\theta_1) + \cos(13\theta_2) + \cos(13\theta_3) + \cos(13\theta_4) + \cos(13\theta_5) = 0 \end{cases} \tag{3}$$

3.2. Formulation of the problem

For each multi-level inverter, an appropriate objective function can be defined as Equation (4), [12]:

$$\mathrm{f} = \min_{\theta_i} \left\{ \left(100 \frac{\mathrm{v}_1^* - \mathrm{v}_1}{\mathrm{v}_1^*} \right)^4 + \sum_{s=2}^{S} \frac{1}{h_s} \left(\frac{\mathrm{v}_{h_s}}{\mathrm{v}_1} \right)^2 \right\} \tag{4}$$

Where in this objective function, the obtaining switching angles is $0 \leq \theta_i \leq \pi/2$. In this function, v_1^* is the desired amount of main harmonic and h_s is rank harmonic remaining in output of the multi-level inverter [12]. Here, the purpose is to find switching angles while at the same time the basic harmonic reaches to the desired amount v_1^* .

According to IEEE-519 Standard, it is recommended that we limit amount of each unique harmonic to 3% of amount of basic harmonic. Therefore, the second part of the above equation avoids the harmonics which are less than 2% of the basic amount. But when a harmonic exceeds from this limit, objective function controls it because of having square power. Finally, rate of each harmonic is added to objective function by a coefficient with the size of that harmonic's reverse rank as weight. By this weighting method, low-rank harmonics lose their high significance.

4. Imperialist Competition Algorithm

Similar to other evolution algorithms, ICA [13-14] begins with an initial population, as well. Members of the population who are in these countries are divided into two categories: colonies (dominions) and emperors (imperialist) which with each other make an empire. The competition between the formed empires is the base of the proposed evolution algorithm. During this competition, the weakest emperor is eliminated and the strongest emperor captures colonies of that empire. Figure (7) shows the proposed algorithm's flowchart. Each emperor who cannot win this competition and cannot increase his power (or at least cannot prevent decrease of his power) will be eliminated in the competition. Steps of imperialist competition algorithm:

Step1. Generating initial empires in algorithm:

In an optimization problem with dimensionsN_{var}, a country as an array of $1 \times N_{var}$ by Equation (5) becomes as Equation (5):

$$country = [P_1, P_2, P_3, \dots, P_{N_{var}}] \quad (5)$$

Cost of each country is obtained by estimating expense function f in amounts ($P_1, P_2, P_3, \dots, P_{N_{var}}$) from Relation (6):

$$cost = f(country) = f(P_1, P_2, P_3, \dots, P_{N_{var}}) \quad (6)$$

Equation (7) shows division of colonies among empires with normalized cost of each empire:

$$C_n = c_n - \max_i\{c_i\} \quad (7)$$

The total normalized cost of all the empires to obtain he possession probability for each empire by equation (8):

$$p_n = \left| \frac{c_n}{\sum_{i=1}^{N_{imp}} c_i} \right| \quad (8)$$

In the equation (9) the number of each of the original colonies against the Empire will be:

$$N.C_n = round\{p_n.N_{col}\} \quad (9)$$

Where $N.C_n$ is initial number of colonies of nth empire and $N_{col}$is total number of colonies.

Step2. Movement of colonies toward empires:

At here, by the movement of colonies toward empire we make a model. This movement is indicated in Figure (8) which colony's new position is shown in bald. At here, the colony has moved toward emperor as much as x unit. Direction of colony's movement toward emperor is a vector. In this figure, x is a random

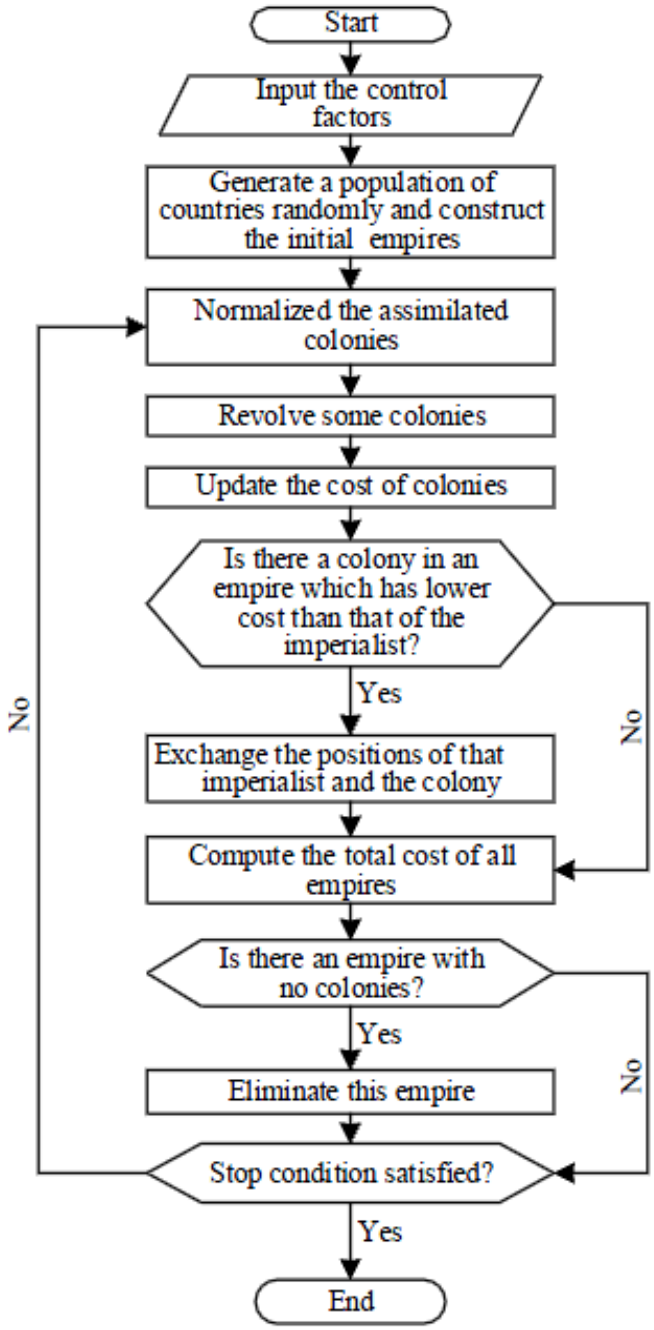

Figure 7. Imperialist Competition Algorithm flowchart [15]

Amount with an uniform distribution. Therefore, for each x we will have Equation (10):

$$x \sim U(0, \beta \times d) \quad (10)$$

Where β*an amount is* greater than one and d is the distance between colony and empire. $\beta > 1$ Causes colonies select an amount in a situation in the neighborhood of situation of empire. To reach different points around empire, we add a random amount from deviation to direction of colony's movement which in Figure (9) this deviation is indicated that θ is a random amount with a uniform distribution which is shown in Equation (11):

$$\theta \sim U(-\gamma, \gamma) \quad (11)$$

γ is a parameter which regulates deviation from the initial direction . However, amounts of β and γ are arbitrary.

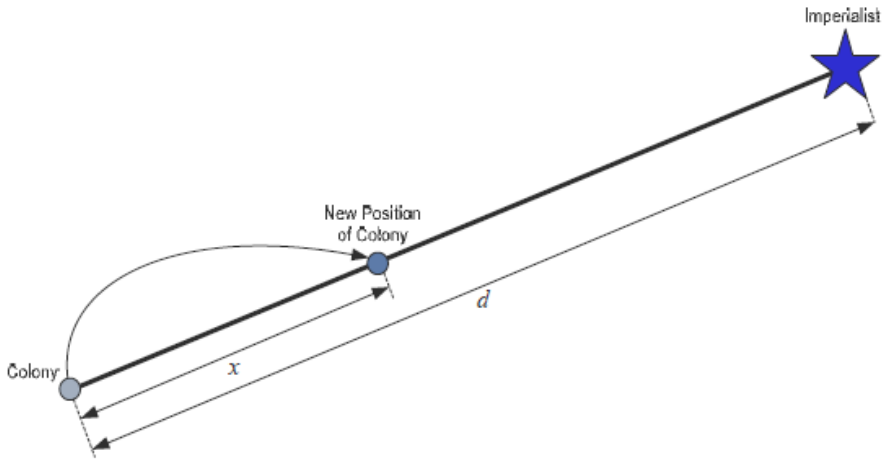

Figure 8. Movement of colonies toward their emperor [14]

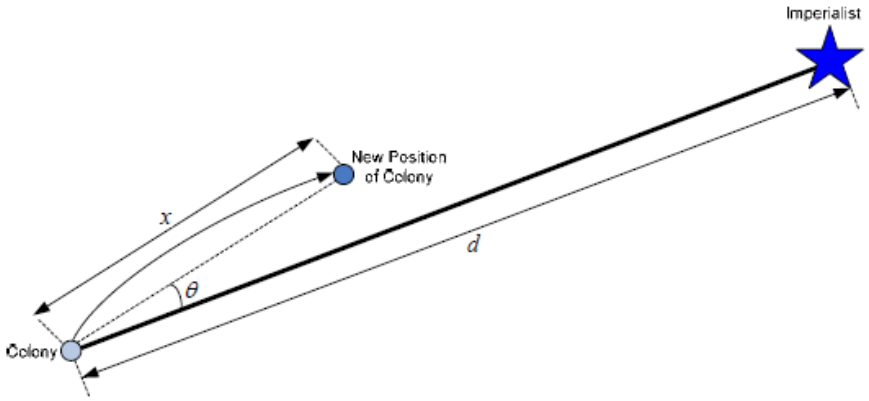

Figure 9. Movement of colonies toward their emperor in a direction with a random deviation [14]

Step3.Change of positions of imperialist and colony (Revolution):

When colonies move toward emperor, it is possible that a colony reaches a situation which has less expense than its emperor. In this case, colony captures position of its emperor and introduces itself as the new emperor of that empire. This case is called Revolution. After revolution, colonies start to move again to go to their new empire. This trend continues until no colony is found that can have less expense in its position than the empire. This step is called intra-group or intra-empire competition.

Step4. Total power of each empire:

Total power of each empire mostly is affected by power of imperialist countries. Also, colonies have insignificant effect on total power of empire. We indicate this fact by defining total cost [16] as Equation (12):

$$Total\ Cost = Cost(imp_n) + \xi * mean * \{Cost(colonies\ of\ empire_n)\} \quad (12)$$

Where ξ is a positive amount between zero and one, small amount for ξ causes total expense mostly be dependent on emperor's expense and its increase causes increase of colonies' role in amount of total expense. In most of application, 0.1 is selected forξ.

Step5. Inter-empire competition:

This imperialistic competition gradually decreases power of the weak empire and increases power of the stronger empire. This competition is modeled just by selecting a number of the weakest colonies of the weakest empires and making a competition among all of empires to capture these colonies. Figure (10) indicates a great image of the modeled imperialist

competition.

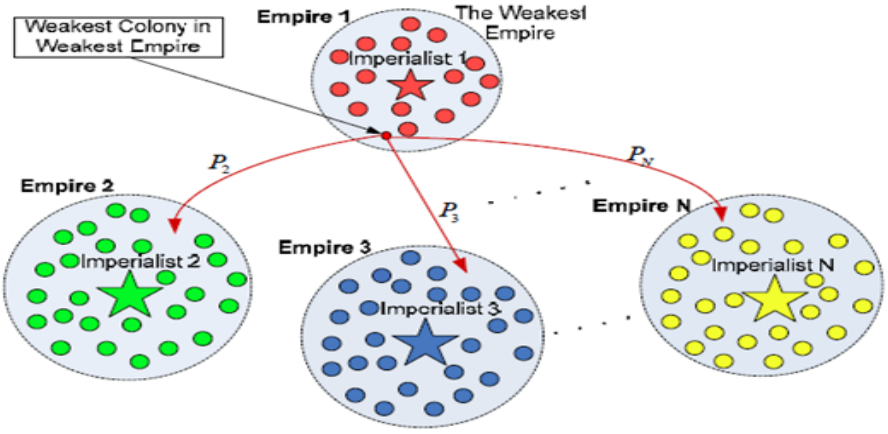

Figure 10.shows that in an imperialist competition, the strongest empire has the most chance to Capture the weakest colonies of the weakest empire [14]

Total normalized cost is obtained by equation (13):

$$N.T.C_n = T.C_n - \max_i\{T.C_i\} \quad (13)$$

Where $T.C_n$ and $N.T.C_n$ are total expense and normalized total cost of the nth empire, respectively. By having normalized total expense, possibility of occupation of each empire is achieved as Equation (14):

$$p_{p_n} = \left|\frac{N.T.C_n}{\sum_{i=1}^{N} N.T.C_i}\right| \quad (14)$$

To divide the mentioned colonies among empires, we form vector P as Equation (15) according to their occupation possibility:

$$P = [p_{p_1}, p_{p_2}, \dots, p_{p_{N_{imp}}}] \quad (15)$$

Then, we make a vector as long as vector P whose elements are random figures which are distributed uniformly that is shown in Equation (16):

$$R = \left[r_1, r_2, \dots, r_{N_{imp}}\right], r_1, r_2, \dots, r_{N_{imp}} \sim U\ (0\ ,1) \quad (16)$$

By subtracting P from R, Equation (17) is obtained:

$$\mathrm{D} = \left[p_{p_1} - r_1, p_{p_2} - r_2, \dots, p_{p_{N_{imp}}} - r_{N_{imp}}\right] \quad (17)$$

Referring to vector D, we will find final occupied colonies which its related index in D has the greatest amount.

Step6. Elimination of empires without colony:

The empires with no power will be eliminated in the competition among imperialists and their colonies will be divided among empires. In modeling elimination mechanism, one can define various criteria to consider empires without power. In most of applications, we assume that an empire is eliminated and removed when it has no colonies.

Step7. Convergence:

When all the empires are eliminated except for the strongest one and all of their colonies are

dominated by that empire, in this new ideal world all the colonies will have the same expense and position and all of them will be controlled by an empire with the same expense and position. In this ideal world, not only there will not be any difference between colonies, but also there will not be any difference between colonies and emperors. In such conditions, imperialist competition finishes and the algorithm is ended.

5. Case study

In this case study, we investigate seven- and eleven-level inverters with even independent dc resources and subsequently we try to eliminate the 5^{th} and 7^{th} harmonics for a seven-level inverter and 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonics for an eleven-level inverter. To implement the proposed algorithm, we consider a statistical population with about 50 countries among which 10 countries are considered as emperors and others as colonies. Then, by applying objective function and the parameters coming from Table 1, the algorithm is implemented. After implementing the algorithm, positions of the obtained angles are checked so that they place in the intended limit which at here is defined as 0 to 90 degrees. And because the obtained angles should be ascendant, in assimilation step angles are defines as following, which firstly the initial angle is considered in 0 to 90 degrees limit and next angle is taken bigger than the previous angle and less than 90 degree into account and then this trend continues until the last angle is found. Because in the objective function we define different switching angles are obtained for different M's, we achieve optimal responses for 7- and 11-level inverters by applying different modulation indexes to algorithm. Figures (11) and (12) indicate amounts of objective function according to index of modulation in interval (1-0) with step 0.01.

Table1. Parameters of imperialist competition algorithm.

nVar	3	Number of Decision Variables for 7 level inverter
nVar	5	Number of Decision Variables for 11 $level\ inverter$
VarMin	0	Lower Bound of Variables
$VarMax$	90	$Upper\ Bound\ of\ Variables$
MaxIt	200	Maximum Number of Iterations
nPop	50	Population Size
nEmp	10	Number of Empires/Imperialists
α	1	Selection Pressure
β	2	Assimilation Coefficient
pRevolution	0.2	Revolution Probability
ν	0.3	Revolution Rate
ζ	0.05	Colonies Mean Cost Coefficient

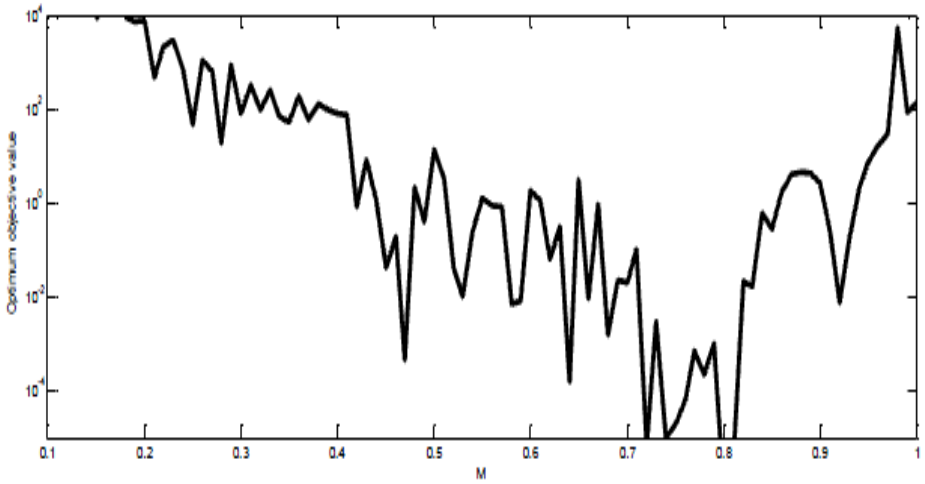

Figure.11. An optimal amount of objective functions according to M for a seven-level inverter.

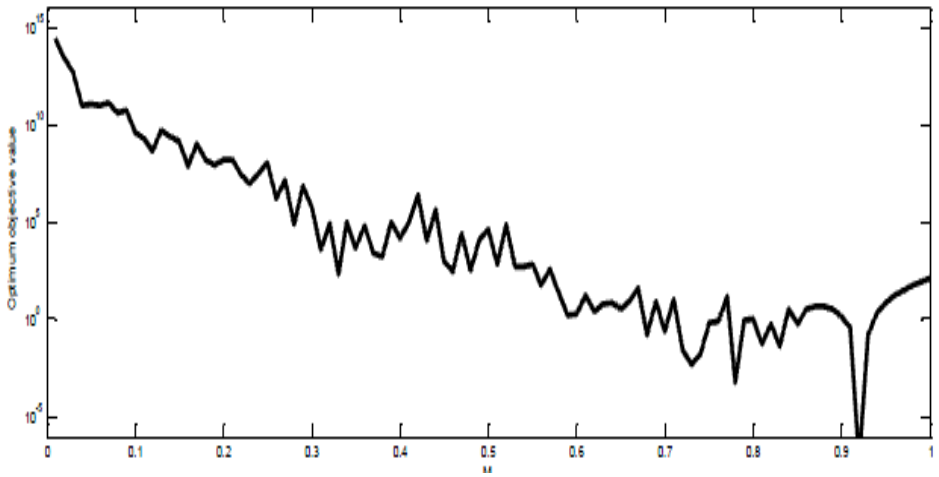

Figure .12.An optimal amount of objective functions according to M for an eleven-level inverter.

Cumulative Distribution Function (CDF) explains this possibility that real amount of random variable X will be in amount less or more than x with a probable distribution, i.e. it can be shown as Equation (18):

$$CDF(x) = P(X < x) \tag{18}$$

At here, the possibility to reach an amount equal or less than the amount of objective function is indicated with CDF curve. For example, $CDF(10^{-2})$ is about 95% for imperialist competition algorithm in a seven-level inverter. That is, the possibility that amount of objective function is less than or equals 10^{-2} is 95%. To show impact of imperialist competition algorithm, Genetic Algorithm was used as a reference. To compare, GA is implemented with the parameters similar to ICA. In Figure (13), CDF curve of imperialist competition algorithm is compared to genetic algorithm which it is observed that CDF of imperialist competition algorithm is more than genetic algorithm and this verifies superiority of this algorithm compared with genetic algorithm [12].

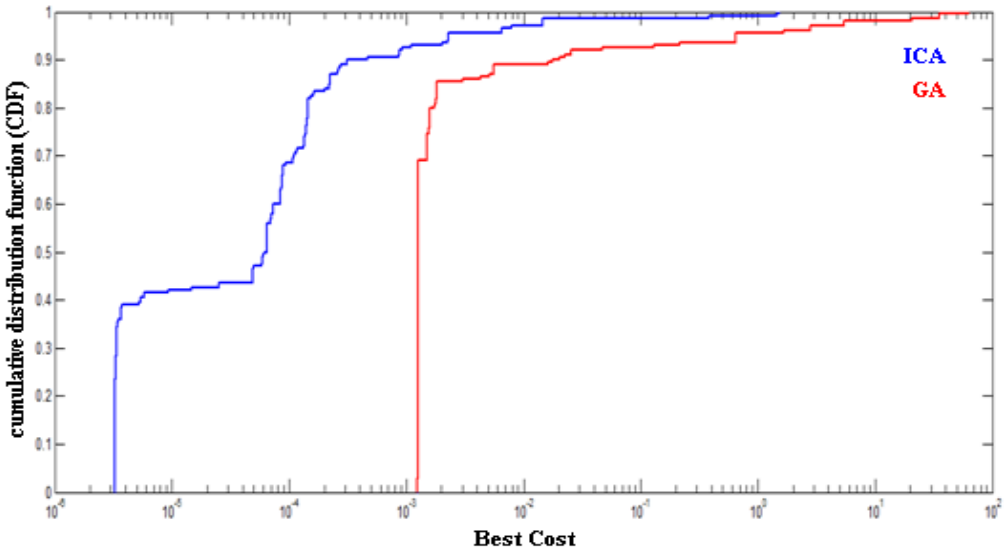

Figure.13. Curve of cumulative distribution functions of ICA and GA

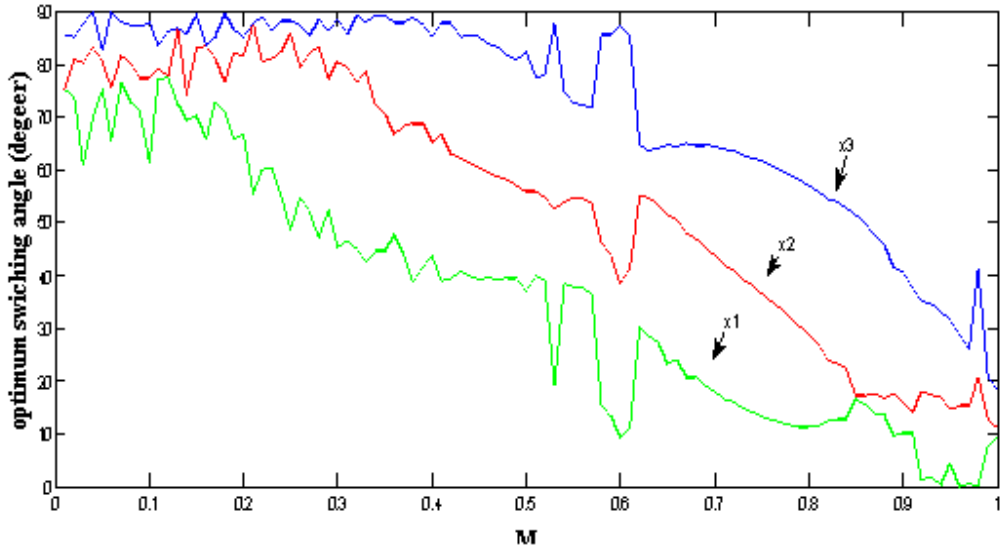

Figure.14. Positions of switching angles according to M for a seven-level inverter

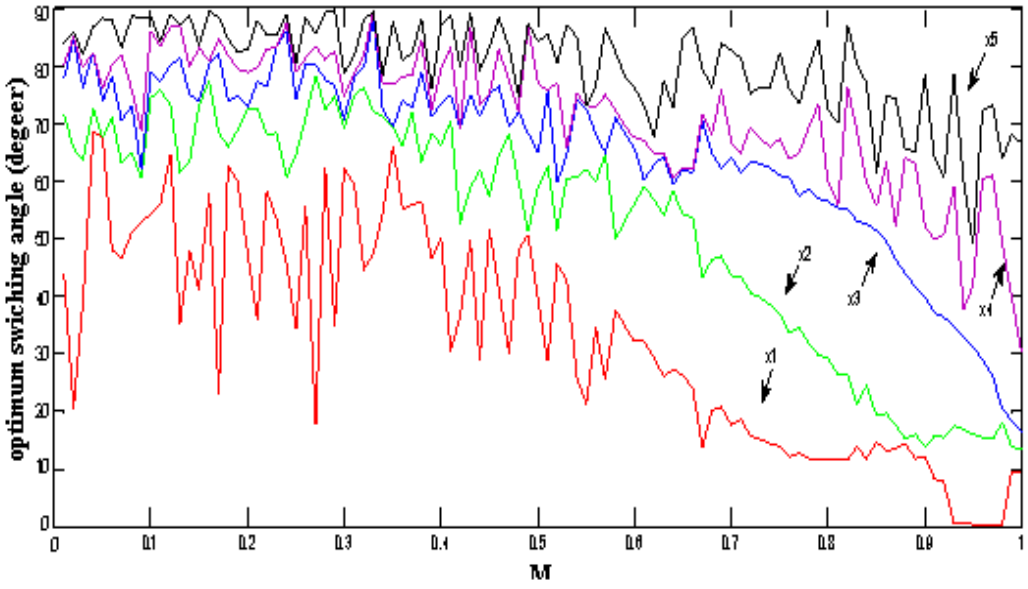

Figure.15. Positions of switching angles according to M for an eleven-level inverter

6. Empirical results

To investigate analyses and results of simulation, the experimental sample of a seven-level inverter made in a laboratory is considered [12]. Each phase of the inverter includes three H-bridge inverter which forms a seven-level waveform. Dc resource of each H-bridge is stable and is considered as 12V. Output power of each inverter with complete bridge can reach to 2kw to 6kw. Finally, total power of the inverter will reach to 18kw. Also, frequency of the output voltage is stable and is considered 50 Hz. Switching angles are obtained by imperialist competition algorithm for different ranges of index of modulation and these angles are loaded in the inverter. Using Simulink software in MATLAB, this inverter was simulated which is shown in Figure (16). For M = 0.8, switching angles are indicated in Table 2 and output voltages resulting from these angles are shown in Figure (17). Figure (18) indicates the frequency range of this waveform which is drawn by FFT analysis in Simulink of MATLAB. It is observed that 5^{th} and 7^{th} low-level harmonics are eliminated in it.

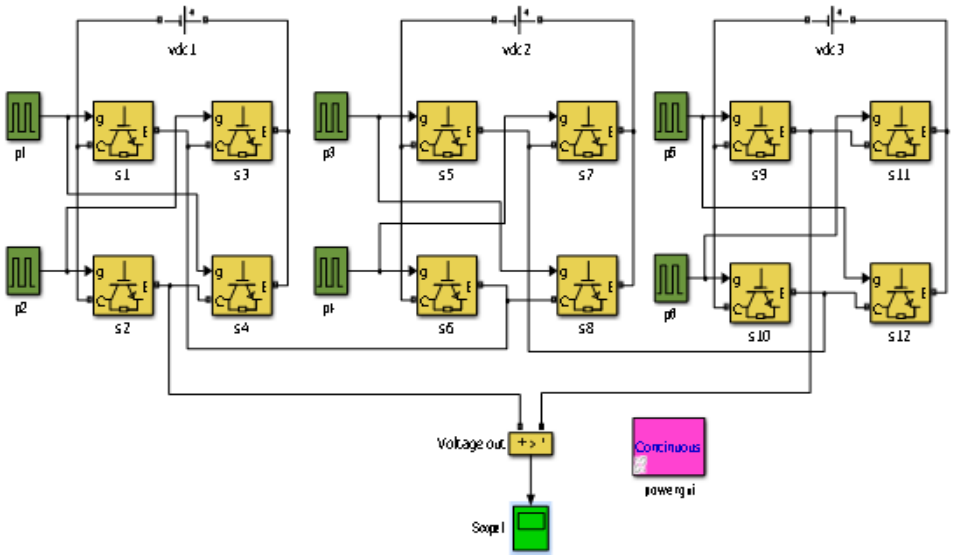

Figure 16. A cascaded seven-level inverter with even independent dc resources

Table 2. Switching angles for M = 0.8

θ_3	θ_2	θ_1	M
57.10	28.71	11.50	0.8

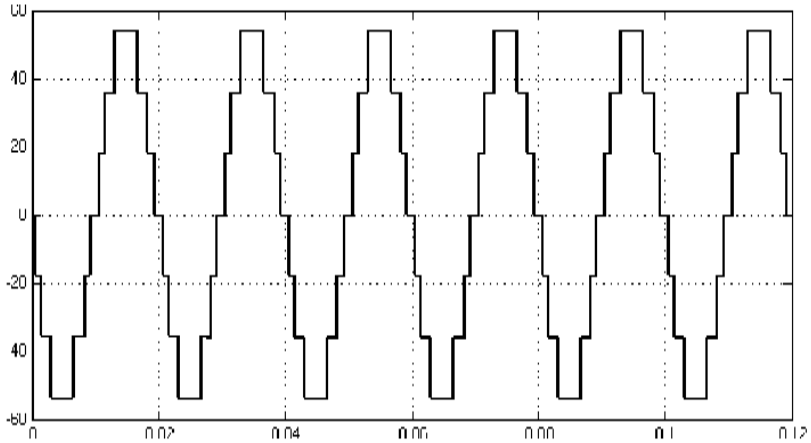

Figure 17. Output phase voltage

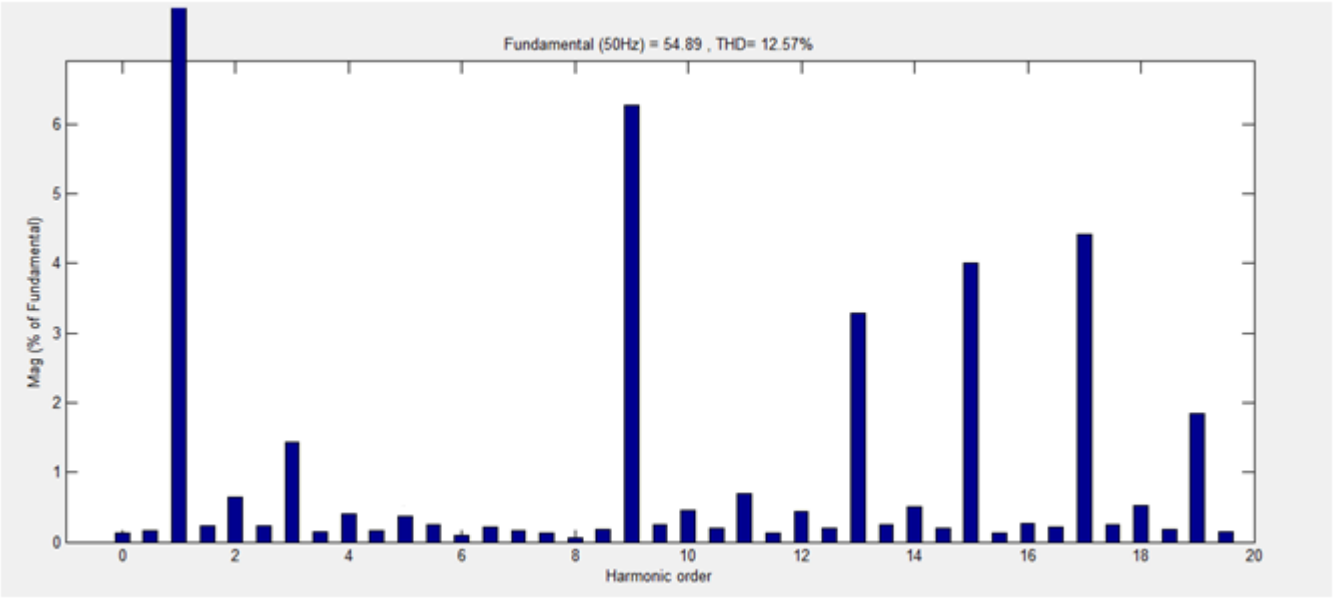

Figure.18. Harmonic range of output phase voltage using FFT analysis

7. Conclusion

In this article, to minimize low-level harmonics in output voltage of multi-level inverters, selective harmonic elimination was used. So optimization techniques are used to solve them .In this regard, the optimum switching angles in order to eliminate low order harmonics is determined through ICA. ICA has been proposed to solve SHE problem with equal DC sources in cascaded multilevel inverter. The proposed method is able to find the optimum switching angles in a simple manner. To optimize switching angle, it is required that non-linear equations be solved. Imperialist competition algorithm was used to solve these equations. Simulation results showed that accuracy and ability of the proposed algorithm is relatively better in convergence and reaching to the least amount. Finally, validity of accuracy of the proposed method was investigated with presented empirical results.

8. References

[1] Karthik, N.,Arul,R. Harmonic Elimination in Cascade Multilevel Inverters using Firefly Algorithm.2014 International Conference on Circuit , Power and Computing Technologies [ICCPCT] (pp. 838-843). IEEE. (2014).

[2] Jeevabharathi, T. P., Padmathilagam,V. Harmonic Elimination of cascaded Multilevel Inverters using Particle Swarm Optimization.2012 International Conference on Computing,Electronic and Electrical Technologies [ICCEET] (pp. 301-306). IEEE. (2012).

[3] J. Rodriguez, J. S. Lai, and F. Z. Peng.Multilevel Inverters: Survey of Topologies, Controls, and Applications. IEEE Transactions on Industry Applications.vol. 49, no. 4. (pp. 724–738). IEEE(2002).

[4] Mariusz Malinowski, K. G. A Survey on Cascaded Multilevel Inverters.IEEE Transaction on industrial electronics, (pp.2197-2206).IEEE (2010).

[5] Leon M. Tolbert, J. N. Elimination of Harmonics in a Multilevel Converter. IEEE Transaction on industrial electronics, (pp.75-82).IEEE. (2005).

[6]] Faete Filho, H. Z. Adaptive Selective Harmonic Minimization Based on ANNs for Cascade Multilevel Inverters With Varying DC Sources. IEEE Transaction on industrial electronics. (pp.1955-1962). IEEE . (2013).

[7] Saravanakumar, R., Anusuya,R.M., Kavitha,V., Gopi,A. Selective Harmonic Elimination in Seven Level Cascaded inverter. 2013 International Conference on Renewable Energy and Sustainable Energy [ICRESE,13] (pp. 51-57). IEEE. (2013).

[8] Mythili, M., Kayalvizhi,N. Harmonic Minimization in Multilevel Inverters using Selective Harmonic Elimination PWM Technique.2013 International Conference on Renewable Energy and Sustainable Energy [ICRESE,13] (pp. 70-74). IEEE. (2013).

[9] Branko L . Dokic, Branko Blanusa . Power Electronics : Converters and Regulators . Berlin: springer. (2015).

[10] J. S. Lai and F. Z. Peng. Multilevel Converters – A New Breed of Power Converters. IEEE Transactions on Industry Applications.vol. 32.(pp. 2348–2356). IEEE (1996) .

[11] Wu, B. High-power converters and ac drive. John Wiely & Sons Ins.s. Hobohen , New Jersey. (1975) .

[12] Kavousi, A.,Vahidi,B., Salehi,R., Bakhshizadeh,M.K., Farokhnia,N., Fathi,S.H. Application of Bee Algorithm for Selective Harmonic Elimination Strategy in Multilevel Inverters. IEEE Transactions on Power Electronics, (pp.1689-1696).IEEE. (2012).

[13] Esmaeil Atashpaz-Gargari, C. L. Imperialist Competitive Algorithm :An Algorithm for Optimization Inspired by Imperialistic Co mpetition. Computation, 2007. CEC 2007. IEEE Congress on (pp. Evolutionary 4661 - 4667). Singapore: IEEE. (2007).

[14] Mohammad A. Al Dossary, Hadi Nasrabadi,'' Well placement optimization using imperialist competitive algorithm'',Journal of Petroleum Scienceand Engineering 147,pp.237–248, (2016).

[15] Mojtaba Mokhtarian Asl, Javad Sattarvand, '' An Imperialist Competitive Algorithm for Solving the Production Scheduling Problem in Open Pit Mine'', IJMGE,Vol 50 ,No 1,pp.131-143,(2016).

[16] Atashpaz-Gargari, E. and Lucas C. (2007). Imperialist competitive algorithm: an algorithm for optimization inspiredby imperialistic competition. in Evolutionary computation, 2007. CEC 2007. IEEE Congress on. IEEE,pp. 4661-4667.